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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,076	08/15/2001	Dean Liu	03226.114001;P6325	9579

32615 7590 02/22/2005

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EXAMINER	
DU, THUAN N	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,076	LIU ET AL.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment (dated 11/22/04) and Drawings (dated 1/21/05).

2. Claim 4 has been cancelled. Claims 1-3 and 5-12 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "the power supply" in line 7. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 2, 3, 5 and 6 are also rejected for incorporating the above deficiency by dependency.

Claim Rejections - 35 USC § 103

8. Claims 1-3 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. [Watanabe] (U.S. Patent No. 5,172,330) in view of Nguyen et al. [Nguyen] (U.S. Patent No. 6,025,616).

9. Regarding claim 1, Watanabe teaches an apparatus comprising:

an integrated circuit [integrated circuit 45 of Fig. 4; col. 3, lines 11-13; col. 4, line 23];

chip logic disposed on the integrated circuit (logic circuit area 44 of Fig. 4 or logic circuit area 124 of Fig. 12) [col. 3, line 21; col. 4, line 28]; and

a clock tree, disposed on the integrated circuit (one or more clock buffers forming a clock tree) [Figs. 4-10; col. 4, line 27], that comprises at least one clock driver [clock buffer 42 of Fig. 4; clock buffer 1205 of Fig. 12; col. 3, lines 25-26], wherein power distributed to the clock tree is isolated from power distributed to the chip logic [Fig. 12; col. 4, lines 25-28].

Watanabe does not explicitly show that the apparatus including a chip package. However, Watanabe teaches that the integrated circuit is electrically connected to external terminal. One of ordinary skill in the art would have recognized that Watanabe's integrated circuit should be housed.

Nguyen shows that in a power distribution system for an integrated circuit comprising:

an integrated circuit (chip 2) [Fig. 1; col. 1, line 62]; and

a chip package (package 8) housing the integrated circuit [Fig. 8; col. 1, lines 65-66];

wherein the integrated circuit is electrically connected to the chip package (bond pads 5 and 7 of chip 2 are electrically connected to external terminals 10 and 12 respectively of the chip package 8) [Fig. 1; col. 1, line 62 to col. 2, line 3].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to recognize that the integrated circuit taught by Watanabe is housed by a chip package and is electrically connected to the chip package as described by Nguyen.

Watanabe shows that the power distributed to the clock tree is isolated, on the integrated circuit, from the power distributed to the chip logic. The integrated circuit is disposed on or housed by a chip package. Therefore, the power distributed to the clock tree is isolated, in the chip package, from the power distributed to the chip logic.

10. Regarding claim 2, Watanabe teaches that a capacitor is coupled along the clock tree [col. 5, lines 19-20]. Since power distributed to the clock tree is isolated from power distributed to the chip logic, power distributed to the capacitor coupled along the clock tree is also isolated from power distributed to the chip logic.

11. Regarding claim 3, even though not shown by Watanabe, however, the logic circuit area 124, inherently, comprises at least one logic element.

12. Regarding claim 5, Watanabe teaches the apparatus further comprising:

a first lead through a circuit board to the computer chip (line 1202), wherein the first lead is used to distribute power from the power supply to the clock tree [Fig. 12; col. 4, lines 26-28]; and

a second lead through the circuit board to the computer chip (line 1201), wherein the second lead is used to distribute power from the power supply to the chip logic [Fig. 12; col. 4, lines 25-26].

13. Regarding claim 6, Nguyen teaches that leads (14) are used to distribute power to the integrated circuit (2), wherein the leads run through the chip package (8) [Fig. 1].

14. Regarding claims 7-12, since they recite method of operating of the apparatus defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday and Wednesday-Friday: 9:30 AM - 8:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (703) 872-9306.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
February 15, 2005